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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,454	11/30/2004	Jean-Jacques Bouny	SC0987ET	1353
23125	7590	10/05/2006	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			WONG, ALAN	
		ART UNIT	PAPER NUMBER	
			2817	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/517,454	BOUNY, JEAN-JACQUES	
	Examiner Alan Wong	Art Unit 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 August 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-11 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-5 and 7-11 is/are rejected.
- 7) Claim(s) 6 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn (US 6,211,734).
3. With respect to claim 1, Ahn discloses an active distortion signal generating circuit (Figure 4) read as pre-distorter to compensate distortions appears in the output of a power amplifier having an operating frequency in the radio frequency (Col. 3 line 32), the characteristics of said power amplifier comprising a distortion from a linear transfer function (Col. 1 line 7-9), said active distortion signal generating circuit comprising a non-linear path 43, a linear path 42, input means (41, 47) responsive to an amplifier input signal for applying respective pre-distorter input signals to said paths and combining means (44, 45) for combining a linear signal from said linear path with a non-linear signal from said non-linear path to produce a pre-distorted signal (Col. 5 line 1-13, 51-59), the characteristics of said pre-distorter comprising a distortion relative to a linear transfer function such as to tend to compensate for the distortion of the transfer function of said power amplifier (Col. 5 line 39-42), wherein said input means is arranged to apply said pre-distorter input signals to said paths substantially in relative phase opposition (Col. 4 line 55-63) and said combining means is arranged to combine said

signals from said paths without introducing any significant relative phase difference (Col. 5 line 1-13, 51-59).

4. With respect to claim 5, Ahn discloses said non-linear path comprises a non-linear path amplifier 43a, and a non-linear path attenuator 43b for receiving a signal from said non-linear path amplifier, and said linear path comprises a linear path attenuator 42a, and a linear path amplifier 42b for receiving a signal from said linear path attenuator.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2-4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,211,734) in view of Quan (US 5,412,354).

7. With respect to claim 2, Ahn does not disclose said input means comprises reactive components introducing opposite phase differences of substantially ± 90 respectively relative to said amplifier input signal.

Quan discloses a magic-tee network (Figure 2), which may be used as a divider, can receive an input at node 112 and output at node 54A and 54C by using only the network configuration 50A (Col. 2 line 61 – Col. 3 line 23). The output at node 54A would be 90-degree since it is a quarter wavelength away from the input node 112. The

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output at node 54C would be 270-degree or -90 degree since it is three-quarter wavelength away.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute Ahn's input means (Figure 2 divider 41) with Quan's magic-tee network. The suggestion or motivation would have been in the absence of structural detail of the divider, a known equivalent configuration would have to be used. Also this configuration can obtain the same phase difference as claimed.

8. With respect to claim 3, Ahn does not disclose said input means and said combining means consist substantially of passive components.

Quan discloses a magic-tee network (Figure 2) that is substantially of passive components (transmission lines 90-100, 102-108 are passive components), which may be used as a divider or combiner.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute Ahn's input means (Figure 2 divider 41) and combiner (Figure 2 combiner 45) with Quan's magic-tee network. The suggestion or motivation would have been in the absence of structural detail of the divider and combiner, a known configuration would have to be used.

9. With respect to claim 4, Quan discloses said combining means (magic-tee network) comprises reactive components (transmission lines are reactive components).

Ahn and Quan do not disclose said combining means comprises reactive components, together with a resistive component decoupling said paths. However,

when Quan's magic-tee network is used, resistors would have terminated any unused terminals/ports and decoupling paths with resistive component is realized.

10. With respect to claim 10, Ahn does not disclose the outputs of said input means and the inputs of said combining means each present an impedance substantially matched to 100 Ohms, and the input of said input means and the output of said combining means each present an impedance substantially matched to 50 Ohms.

Quan disclose a magic-tee network (Figure 2) that if only the network configuration 50A is used (Col. 2 line 61-67), the nodes 54A, 54B, and 54C would have 50-ohm impedances (Col. 3 line 9-10) and nodes 110 and 112 would have 100-ohm impedance (Col. 3 line 11-12). This can be use as a divider or combiner.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute Ahn's input means (Figure 2 divider 41) and combiner (Figure 2 combiner 45) with Quan's magic-tee network. The suggestion or motivation would have been in the absence of structural detail of the divider and combiner, a known configuration would have to be used. For divider, the input may enters at node 54B and outputs at node 110 and 112. For combiner, the inputs may enter at node 110 and 112 and outputs at node 54B. Under this configuration, the claimed impedances can be realized.

11. Claim 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,211,734) in view of Hedberg et al. (US 6,731,168).

12. With respect to claim 7, Ahn does not disclose substantially all the components of said pre-distorter are formed in a common semiconductor substrate.

Hedberg et al. disclose a predistortion processor 20 on a common substrate (Col. 6 line 55-58).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to form Ahn's active distortion signal generating circuit (Figure 2) on a substrate as Hedberg et al. had with his invention. The suggestion or motivation would have been easier for implementation and integration.

13. With respect to claim 8, of the combination, Ahn does not disclose components of said power amplifier (Ahn's Col. 5 line 42, not illustrated but mentioned) are formed in said common semiconductor substrate; and with respect to claim 9, of the combination, Ahn does not disclose substantially all the components of at least a first stage of said power amplifier are formed in said common semiconductor substrate.

However, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form Ahn's power amplifier in the said common semiconductor substrate in the combination. The suggestion or motivation would have been easier for implementation and integration.

14. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,211,734) in view of Ghannouchi et al. (US 6,255,908).

15. With respect to claim 11, Ahn does not disclose a variable attenuator interposed between said power amplifier and said active distortion signal generating circuit (read as pre-distorter).

Ghannouchi et al. disclose a linearization circuit (Figure 2) with a variable attenuator 16 between a power amplifier and linearizer 4 (Col. 6, line 12-15).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have an attenuator as in Ghannouchi et al.'s. The suggestion or motivation would have been better control of the input's power applied to the power amplifier as known in the art.

16. Applicant's arguments filed 8/2/2006 have been fully considered but they are not persuasive.

The output of Ahn's active distortion signal generation circuit is able to read as a pre-distortion signal because it is eventually input to the power amplifier to compensation for distortion occur in the power amplifier. Since the signal is before inputting into the power amplifier and helps provide compensation for distortion, it is considered a "pre-distortion signal" by those of ordinary skill in the art. The active distortion generation circuit generates this "pre-distortion signal", thus it is read as a pre-distortion. The paths Ahn referred to "linear" and "non-linear" stand since the paths start after the dividing means (divider 41 and variable attenuator and phase shifter 47) and end at the combining means (44 and 45). The processing subject to the signal output afterward (the combined signal) should not be used to determine the linearity of the paths beforehand. While there is no disclosure of phase difference in the device 21a, the divider means for the input to the pre-distorter (active distortion signal circuit) is device 41 and 47. Together they generate signal outputs for the linear and non-linear path with 180-degree (Col. 4 line 60-63).

Allowable Subject Matter

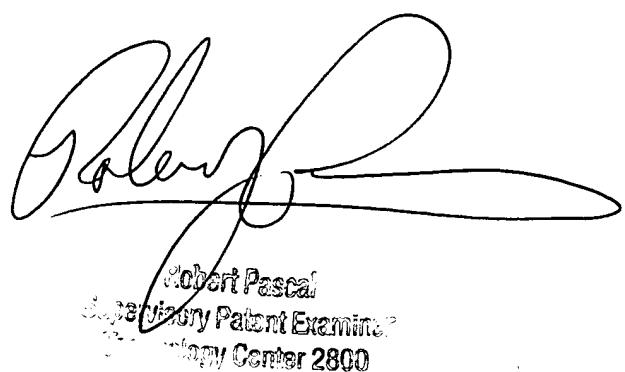
17. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
18. The following is a statement of reasons for the indication of allowable subject matter: With respect to claim 6, no cited references disclose the further limitation on said non-linear path amplifier is arranged to operate at conditions of bias voltage and said linear path amplifier is arranged to operate at similar conditions of bias voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan Wong whose telephone number is (571) 272-3238. The examiner can normally be reached on Mon-Thurs 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bob Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AW



A handwritten signature in black ink, appearing to read "Robert Pascal".

Robert Pascal
Examination Patent Examiner
Priority Center 2800